REMARKS

This amendment is submitted in response to the Final Office Action dated July 20, 2007. Reconsideration and allowance of the claims are requested. In this Final Office Action, claims 1, 2, 5-11, 14, 31, 33 and 34 are rejected under 35 U.S.C. 102 as anticipated by Simmonds (U.S. 6,646,654). Claims 12 and 13 are rejected under 35 U.S.C. 103 as unpatentable over Simmonds. Claim 35 is rejected as unpatentable over Simmonds in view of Itaki (U.S. 6,900,844). These rejections are respectfully traversed.

In response to this Final Office Action, the claims have been amended to emphasize that the present invention is directed to dealing with the problem spelled out in the background of the invention and exemplified in Figure 1, where a plurality of graphic processing units have to be synchronized for controlling image content provided to multiple projectors so that a single image can be displayed in synchronized sections across the different projectors. Such a system requires that each of the graphics processing units be exactly synchronized with the others so that the different portions of the image to be displayed appear synchronously. The above limitations are now recited in the features added to the claims.

The claims further recite that a synchronized display is achieved by transmitting a signal to each of the graphics processing units and adjusting the internal operation of each GPU during data transfers in each GPU by synchronizing the phase of an internal synchronization signal with an externally generated timing signal. As further spelled out in the newly added dependent claims 36 and 37, this result is specifically achieved by performing a series of video memory block transfers in each of the graphics processing units to create the displayed image portions, which are under the control of the internal synchronization signals.

These features are not present in the Simmonds reference. It bears repeating that the system, as claimed, utilizes synchronization signals that are internal to the graphics processing units and are maintained in synchronous phase with an external signal throughout the transmission of the different portions of the image generated by each of the participating graphics processing units. In contrast, in Simmonds, there is no comparison between an external sync signal and the internal clock signals used to

maintain and control the data transfers within each graphics processing unit using the phase synchronize signal. Rather, as shown in Simmonds Figure 5, there is only a master/slave detection system that incorporates PLL 130. The PLL output can only chose between the external signal, if it is determined that the sync card 100 is a slave, or a reference clock oscillator 120, if the card is a master. Specifically, there is no teaching of adjusting an internal clock generator frequency at each graphics processing unit to match in phase an external sync signal to generate a synchronized timing signal within each of the GPUs, as expressly recited in the claims. Simmonds, while teaching that a card may have either an internal clock or an external reference signal, does not teach a comparison between those signals or an adjustment of the phase of the internal clock, which is maintained throughout the operation of the GPU, to control data transfers within the GPU to form a synchronously maintained image.

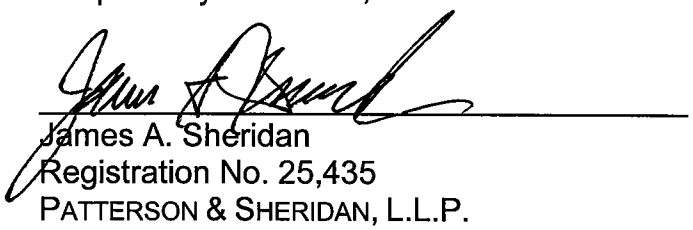
Claims 3, 4 and 32 which teach synchronizing a first stereo field of the GPU with a second stereo field must similarly be allowed. The rejection depends entirely on the Examiner's assumption that Simmonds teaches adjusting the phase of video signals in each of the first and second GPUs. As the Examiner concedes in his Office Action, there is no such teaching within the reference nor does it inherently occur.

Claim 5 and its dependent claims 6-13 and claim 33 also recite allowable subject matter. The Examiner argues that Simmonds teaches synchronizing a swap ready signal of the first GPU with a swap ready signal of the second GPU which is the language found in the claims. But in fact, this is contradicted by column 10, lines 52-67 of Simmonds, which teaches that bumper swap synchronization occurs in a different manner than claimed. Simmonds utilizes a master swap controller connected to all graphics subsystems that determines that an interrupt has occurred at each graphic subsystem. It is only at this time that the swap ready signal can be defined. Thus, Simmonds teaches an inefficient and time consuming process that depends on every GPU being interrupted and the interrupt being maintained so that a bumper swap may occur under the direction of the master controller. In the claimed system, the detection of swap ready signals between first and second GPUs has immediate synchronization scanned out of the data once synchronization as claimed in the independent claims occurs. This is a faster and more efficient approach than that taught by Simmonds.

In the Advisory Action of September 26, 2007, the Examiner urges that in order for the PLL to work, a clock signal must be input to the PLL to be compared and adjusted and that this is shown in Figure 5 of Simmonds. It is agreed that Figure 5 of Simmonds does show a clock signal being input to the PLL. However, it is clearly taught by Simmonds that the output of the PLL goes only to a controlling output selection port of a MUX 122 to chose between two possible clock signals which are used to control each of the graphics subsystems. As shown, at Figure 4, the MUX 122 chooses between one of the two available clock sources. Each GPU will use the external clock source if the graphics subsystem is a slave and an internal clock source from a reference clock oscillator 120 if the system is the master system. However, there is no ongoing adjustment of a clock source signal with the resulting phase adjusted signal being used internally by the GPU to drive data transfers within each of the GPUs. Therefore, as claimed, the claims clearly distinguish over the teachings of the Simmonds reference.

In view of these clear distinctions, reconsideration and allowance of the claims is requested.

Respectfully submitted,



James A. Sheridan
Registration No. 25,435
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicants